10 MHz Buffer to be installed on the HP 10544A board

The basic reasons for adding a separate buffer at the OCXO output were:

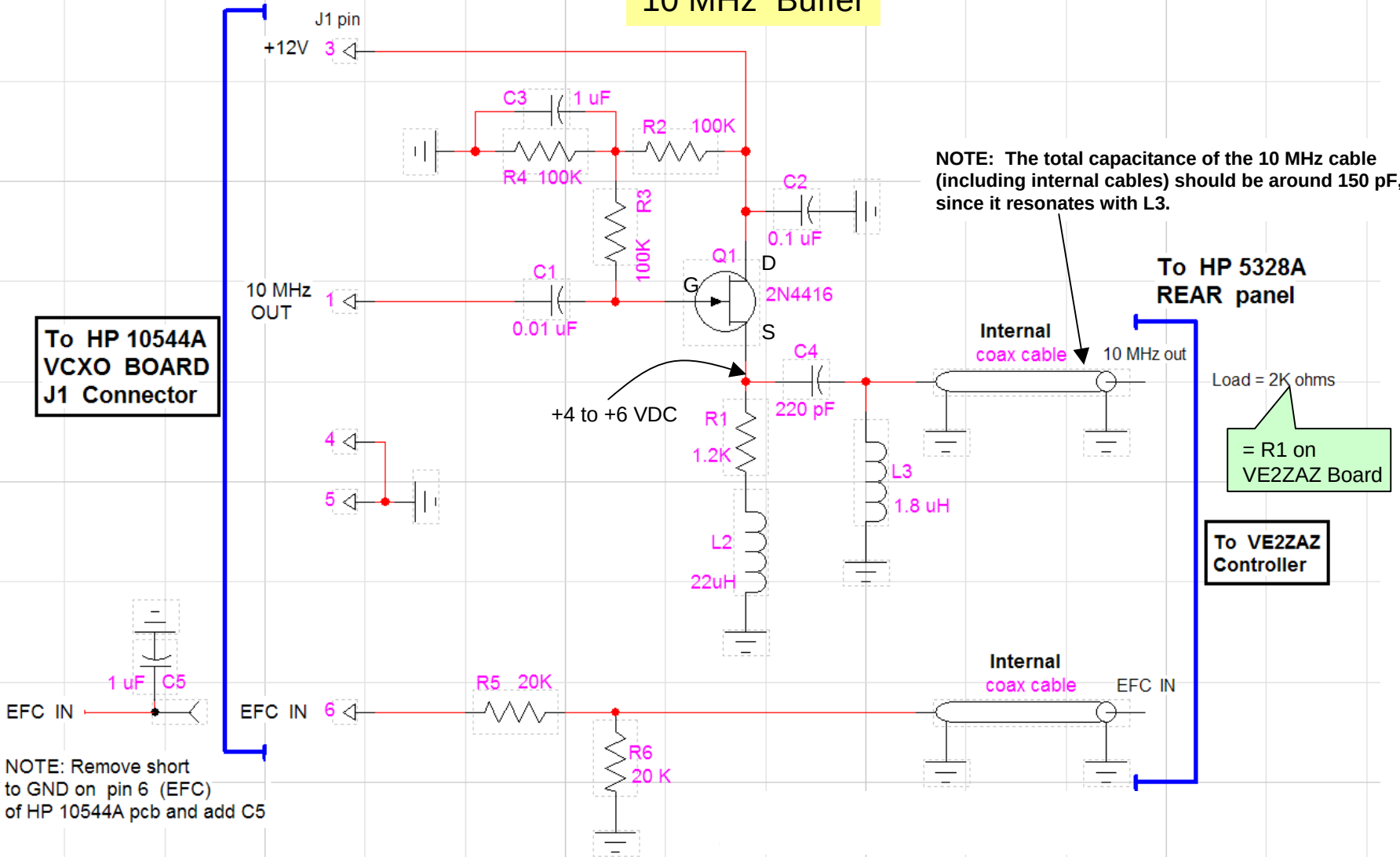
1- To drive the coax cable carrying the 10 MHz signal.

2- To have the 10 MHz available when the counter is in standby mode.
In this mode the rear 10 MHz output is deactivated (all logic circuits are) as well as most other circuits.
Note that my buffer is always on since it uses the OCXO +12V supply.
The normal 10 MHz rear output will work with VE2ZAZ circuit, as it provides more than 4 V p-p.
I noticed that this output has some small DC level jumps on it lasting less than 1 uSec, as a consequence of logic gate switching. However it should not be of any consequence.

Note: If you build Bert VE2ZAZ's circuit inside the counter, then my FET buffer
Is NOT required anymore !
In this case I recommend that you provide a separate supply for Burt's circuit, like an external wall transformer. Insure that the 7805 regulator IC is well heatsinked to the counter chassis to minimize the +5V variations and set the course freq. adjustment to thave the control voltage close to 0 V.

See also the last page.

10 MHz Buffer



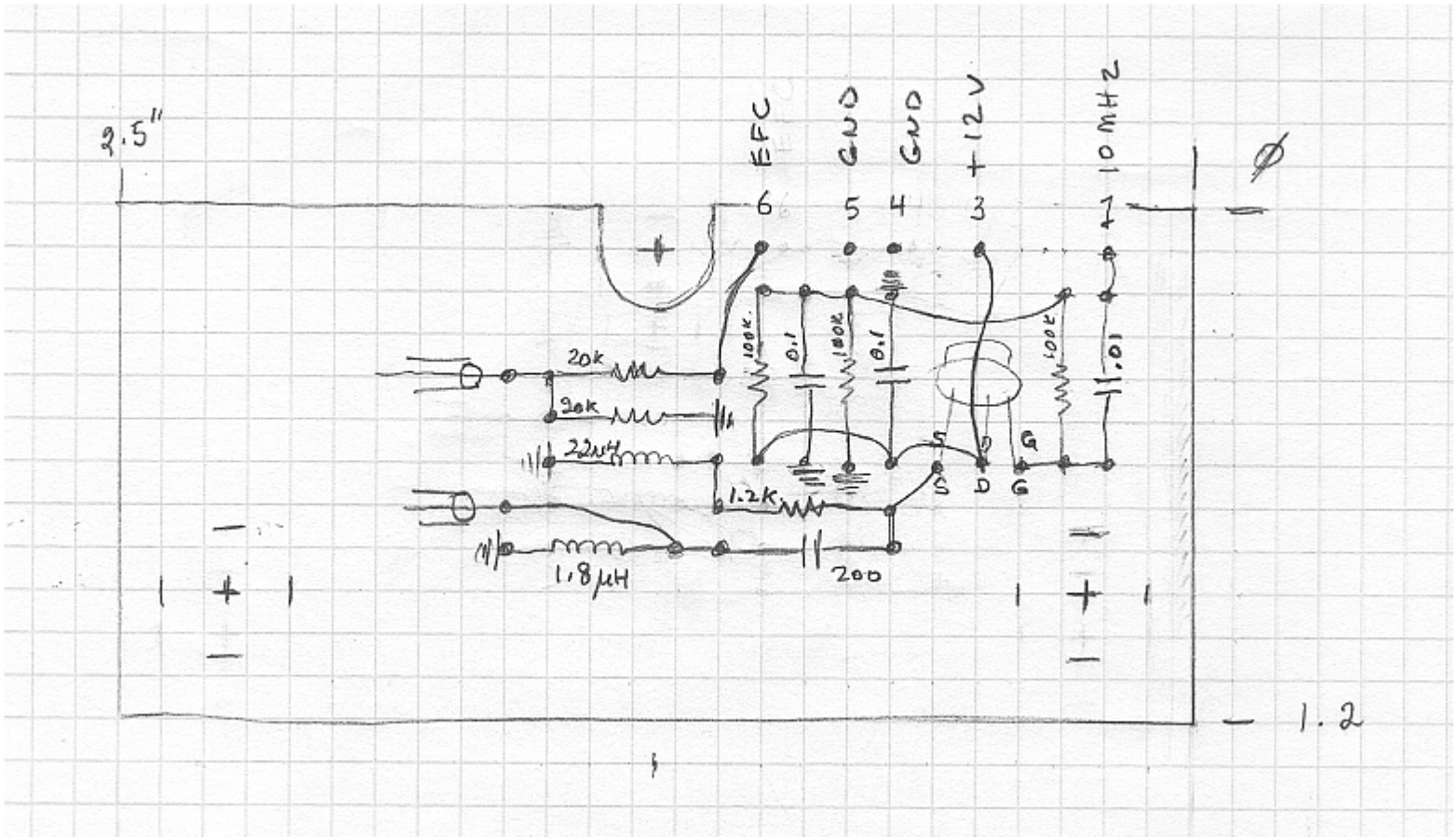
Note: The buffer output uses a low Q resonant circuit that cancels the connecting cable capacitance and provides filtering against possible spurious far away from 10 MHz. This means that the LCT1485 input sees a very clean 10 MHz waveform. The only spurious that I could detect on the 10 MHz output were the heater switching transients at 3.7 KHz and a few multiples. These were - 80 dB down from the carrier, too low to worry about.

10 MHz BUFFER

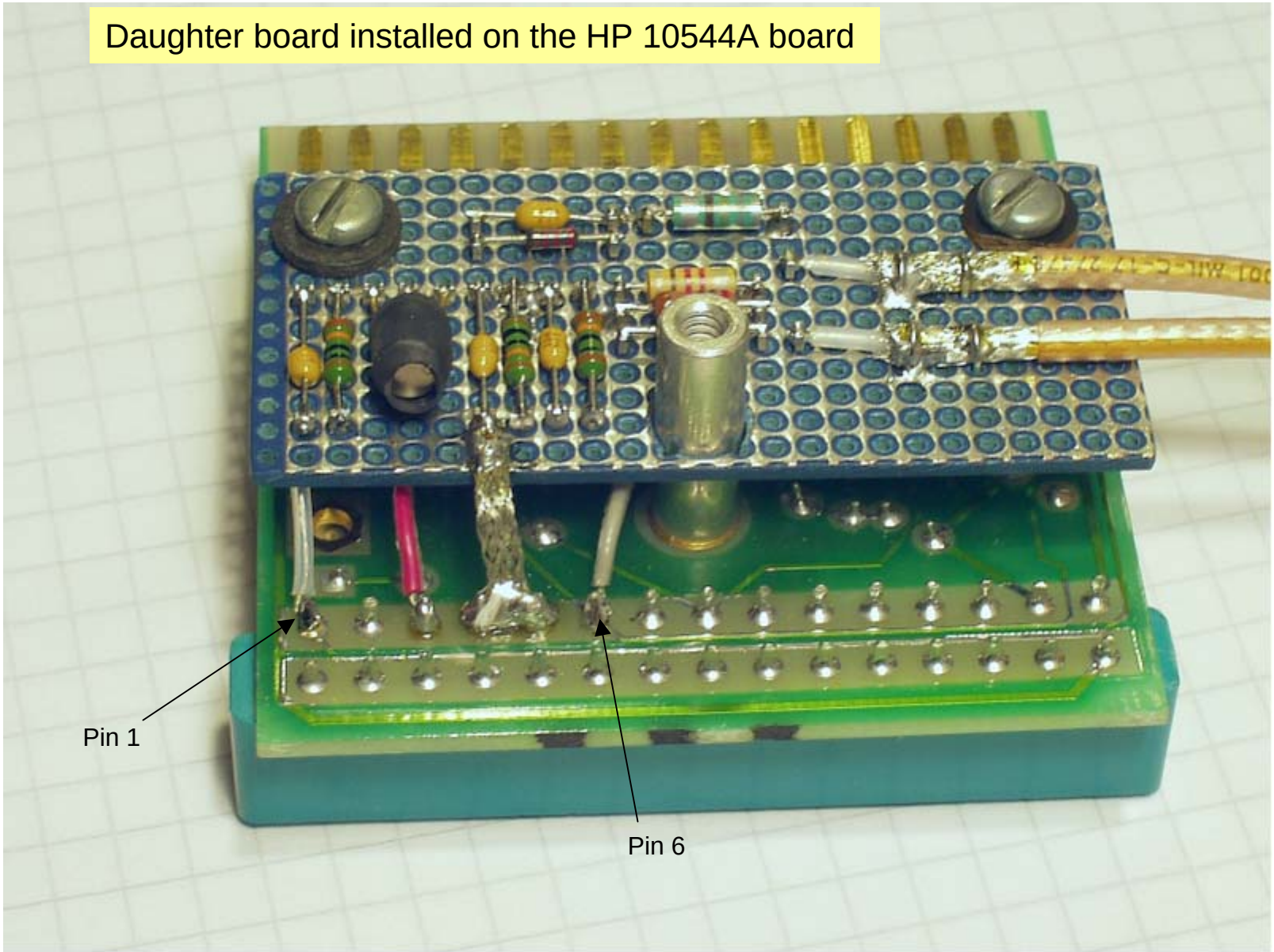
VE2AZX

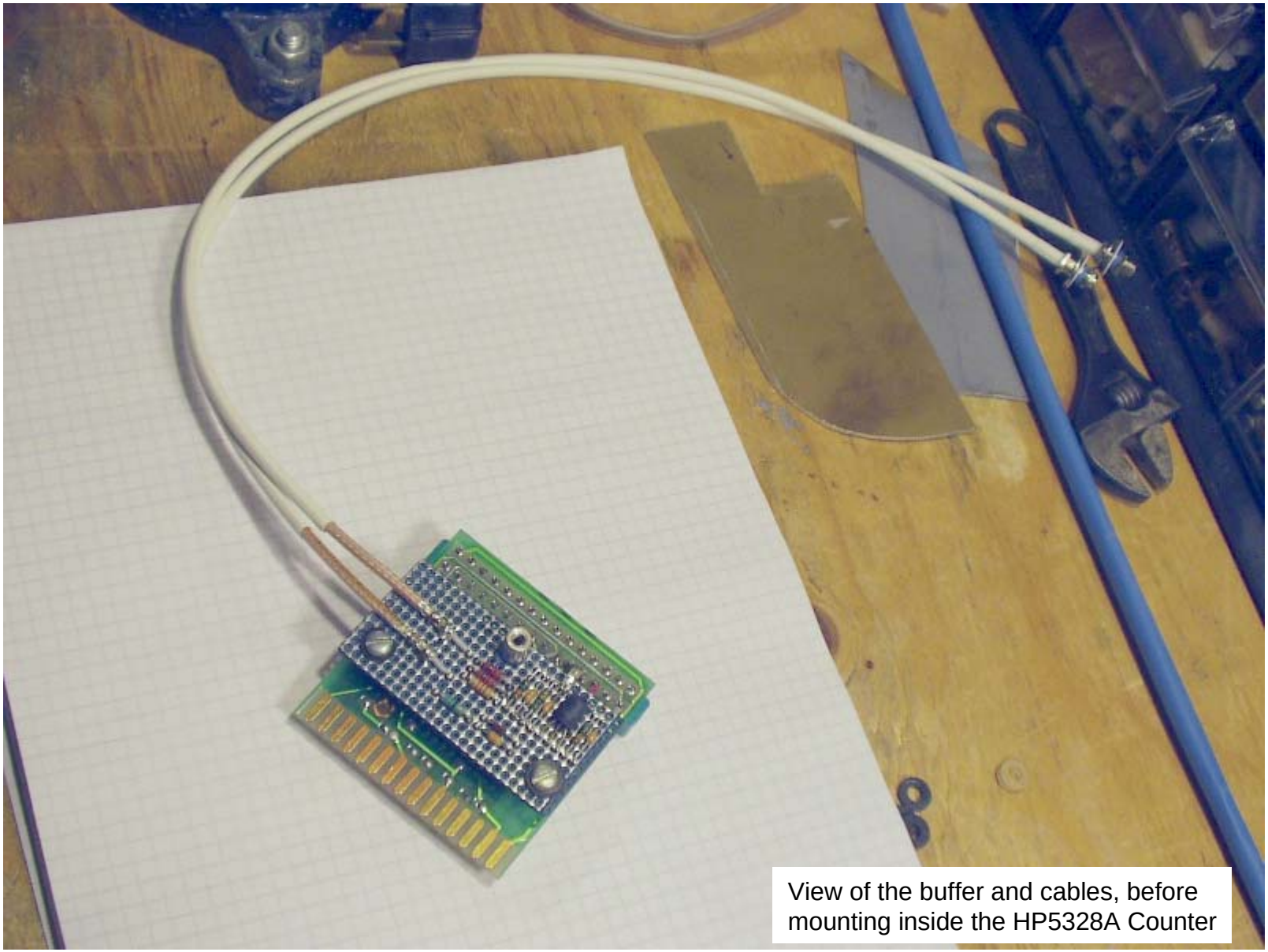
Sketch of daughter board

Drawn to scale



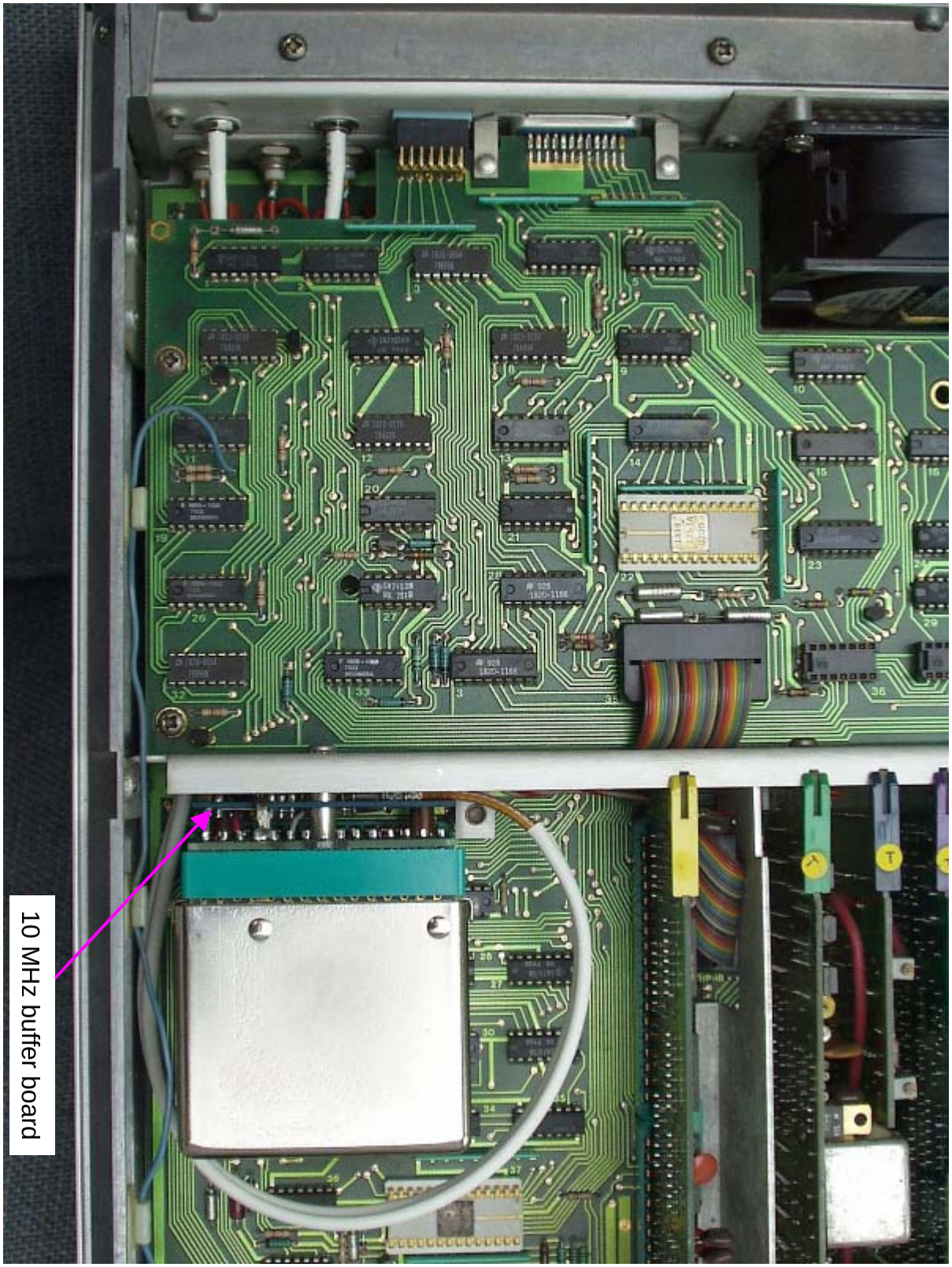
Daughter board installed on the HP 10544A board

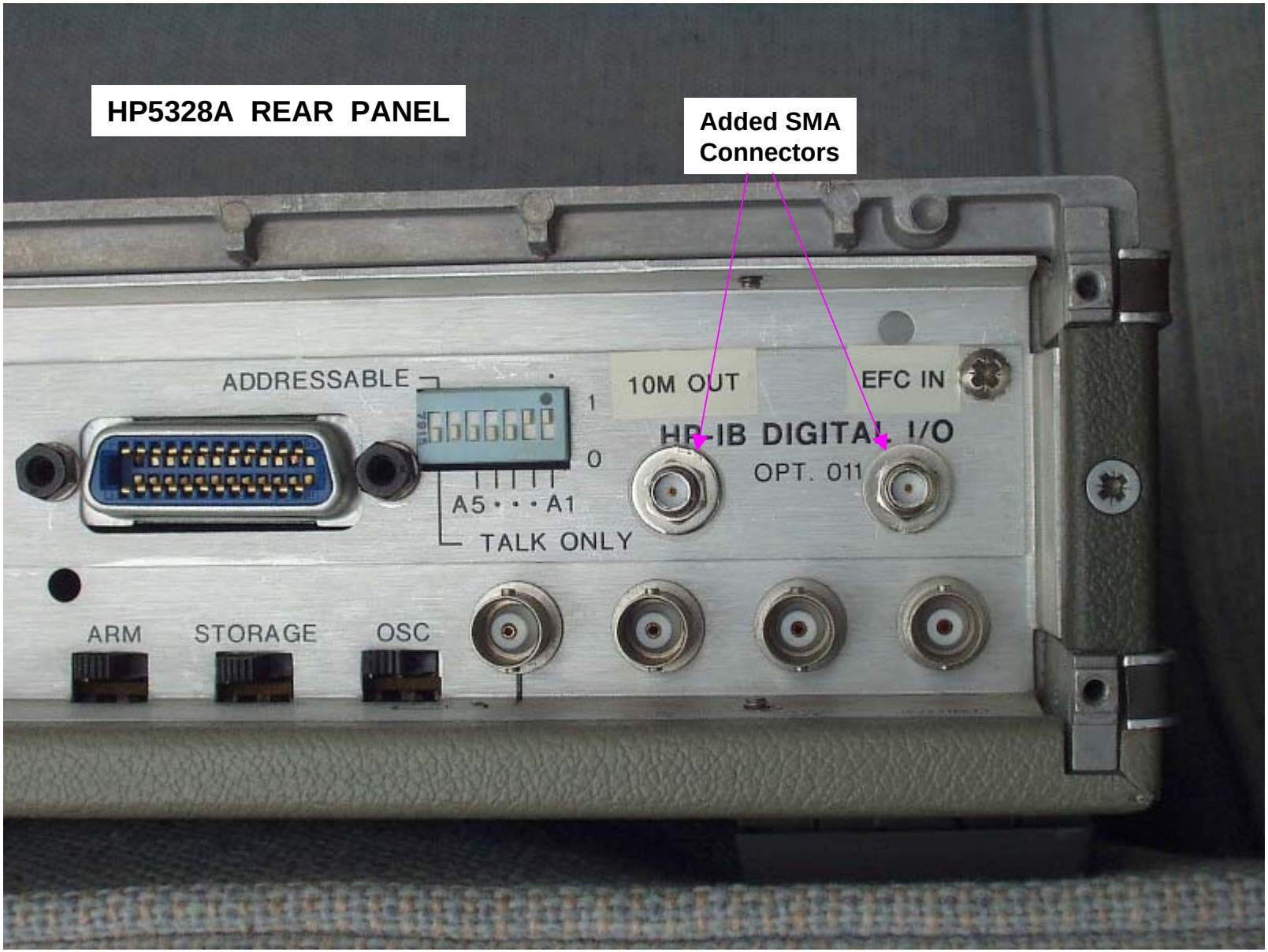




View of the buffer and cables, before mounting inside the HP5328A Counter

HP5328A REAR PANEL




HP5328A REAR PANEL
Added SMA Connectors
ADDRESSABLE
1
0
A5 • • • A1
TALK ONLY
10M OUT
EFC IN
HP-IB DIGITAL I/O
OPT. 011
ARM
STORAGE
OSC

Q & A

Q- How critical are the specs on the JFET 2N4416 ?

A- The J FET is not critical. An MPF102 should be OK, but you might have to select them.
The problem is that their Idss (current Drain to Source with source Shorted) may vary from 2 to 20 mA.
It should be from 3.3 to 8 mA approx. The source voltage on (C4-R1 junction) should be +4 to +6 Volts.
Resistor R1 may be increased to 1.5 K or even 1.8K to accept FETs with lower values of Idss.
The FET should not operate with a gate to source voltage of more than say 0.3V,
otherwise it's internal diode will get forward biased and the FET action will be lost.

Q- What is the purpose of the GPS battery backup ?

A- The backup battery is ONLY used to keep the GPS data (position) memory alive when it is powered off.
There is a pin for battery backup on my Trimble GPS for this purpose.
Loosing the GPS data is not really a problem, it just takes more time to resynchronize next time,
and it gives an alarm on its serial port.

Q- How is the GPS active antenna powered ?

A- The GPS active antenna is powered by its +5V supply, with a current limiting. The GPS detects
when the antenna is disconnected and reports it on the serial port.
You can verify this with a DC voltmeter on the antenna connector.